Customer No.: 31561
Docket No.: 10228-US-PA
Application No.: 10/605,082

AMENDMENTS

In The Claims

Claims 1-8 (cancelled).

Claim 9. (previously presented) A chip structure, comprising:

a die having an active surface and a back surface, wherein the active surface is implemented with a plurality of bonding pads;

an under-bump-metallurgy (UBM) layer disposed over the bonding pads;

a patterned dielectric layer over the active surface of the die, wherein the patterned dielectric layer has a plurality of openings that expose the bonding pads and the UBM layer is disposed above the patterned dielectric layer;

a plurality of solder blocks respectively disposed above the under-bump-metallurgy layer; and

a passive component having a plurality of terminal electrodes, wherein at least two terminal electrodes are respectively disposed at two ends of the passive component, and the terminal electrodes are respectively coupled to the UBM layer through the solder blocks.

Claim 10. (cancelled).

Claim 11. (original) The chip structure of claim 9, wherein the UBM layer further comprises a re-distribution layer and the re-distribution layer is electrically connected to the bonding pads.

Claim 12. (original) The chip structure of claim 9, wherein the under-bump-metallurgy

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layer is a composite metallic layer.

Claim 13. (previously presented) A chip package structure, at least comprising:

a substrate having an upper surface;

a die having an active surface and a back surface, wherein the back surface of the die is in contact with the upper surface of the substrate and the active surface is implemented with a plurality of bonding pads;

an under-bump-metallurgy (UBM) layer disposed over the bonding pads;

at least two solder blocks disposed on the under-bump-metallurgy layer;

a passive component with a plurality of terminal electrodes, wherein at least two terminal electrodes are respectively disposed at two ends of the passive component, and the terminal electrodes are coupled to the under-bump-metallurgy layer through the solder blocks;

a plurality of conductive wires electrically connecting the die and the substrate; and

a packaging plastic enclosing the die, the passive component, and the conductive wires.

Claim 14. (original) The chip package structure of claim 13, wherein the UBM layer further comprises a re-distribution layer and the re-distribution layer is electrically connected to the bonding pads.

Claim 15. (original) The chip package structure of claim 13, wherein the under-bump-metallurgy layer is a composite metallic layer.

Claim 16. (original) The chip package structure of claim 13, further comprising a patterned dielectric layer disposed over the active surface of the die with a plurality of openings to expose the bond pads and the UBM layer is disposed above the patterned dielectric layer.

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Claim 17. (new) The chip structure of claim 9, wherein the passive component comprises resistor, capacitor, or inductor.

Claim 18. (new) The chip package structure of claim 13, wherein the passive component comprises resistor, capacitor, or inductor.

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